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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,083	07/10/2001	Motoki Higashida	027260-477	7077

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Platon N. Mandros
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,083	HIGASHIDA, MOTOKI	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This non-final office action is in response to amendments filed on 5/24/05.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] in view of, Tobias et al., US Patent no. 6,363,501 [Tobias].

Regarding claim 1, AAPA teaches a leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region [main power supply region 18, Figure 7] including circuits operated by receiving power from a main power source [main power source 3, Figure 7], and a backup power supply region [backup power supply region 19, Figure 7] including a built-in storage section [built-in SRAM 15, Figure 7] for saving stored content [page 2, paragraph 3].

AAPA does not explicitly teach starting a scanning operation and reading information held in the memory units of each of the circuits provided in the main power supply region when the LSI chip is placed in an operation standby state.

Tobias also teaches a method of reducing power consumption of an LSI chip. Tobias teaches:

connecting memory units [peripheral configuration registers, column 4, lines 19-25] in each of the circuits provided in the main power supply region through a scan path [SCAN_PATH, column 4, lines 25-40];

starting a scanning operation, when the LSI chip is placed in an operation standby state [column 7, lines 22-35], through the scan path, and reading information [configuration data] held in the memory units of each of the circuits provided in the main power supply region [column 4, lines 36-40 and Figure 5]; and

saving the information thus read by the scanning operation [column 7, lines 1-9 and Figure 5].

It would have been obvious to one of ordinary skill in the art to combine the teachings of AAPA and Tobias. Utilizing a scan path to save information held in the memory units of each of the circuits provided in the main power supply region eliminates the need for the execution unit of the LSI to intervene when saving the information before placing the LSI chip into a standby state [Tobias, column 2, lines 52-60]. One of ordinary skill in the art would be motivated to modify the AAPA in view of Tobias because eliminating the need for the execution unit of the LSI to intervene when saving the information will reduce power consumption of the LSI.

AAPA and Tobias, as described above, teach using a scanning operation to save information of memory units before powering down a LSI in order to reduce leakage current. AAPA and Tobias do not specifically state that reading of the information during the scanning operation is based on a scan mode signal and a scanning clock pulse. However, Tobias does state that the scanning hardware is IEEE 1149.1 compliant [column 2, lines 52-60]. IEEE 1149.1 states that compliant scanning hardware must implement a test clock [TCK] and a test mode

select [TMS] signals for controlling operations of the scanning hardware [pages 9-14]. Therefore, AAPA and Tobias do teach that the scanning operation is based on a scan mode signal and a scanning clock pulse.

Regarding claim 2, AAPA states that the built-in memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 3, Tobias teaches saving the scanned information into a separate storage section [external memory 200, column 7, lines 1-9].

Regarding claim 4, AAPA states that the memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 5, Tobias teaches using the JTAG boundary scan path to save configuration data to external memory [column 6, lines 47-63].

Regarding claim 7, AAPA states that the memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Regarding claim 9, AAPA and Tobias do not specifically address presetting a voltage of the backup power source to be lower than a voltage of the main power source, yet enough for holding the content of the storage section provided in the backup power supply region. The examiner takes official notice that operating circuitry at a lower voltage level consumes a lower amount of power. Therefore, it would have been obvious to one of ordinary skill in the art to set the operating voltage of the backup power supply section to the lowest level which still permits the circuitry in the backup power supply region to successfully operate in order to save power in the LSI.

Regarding claim 10, AAPA states that the built-in memory storage section is formed by SRAM [built-in SRAM 15, Figure 7 and page 2, paragraph 3].

Claims 6 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Tobias et al., US Patent no. 6,363,501 [Tobias], in view of, Goldstein, US Patent no. 6,684,275.

Regarding claim 6, Tobias teaches starting the scanning operation, when the LSI chip is placed in the standby state [column 7, lines 22-35], through the scan path, serially reading the information held in the memory units of each of the circuits provided in the main power supply region and saving the thus converted parallel information in specified addresses of the scanned information storage portion of the storage section [column 2, lines 23-27 and column 6, lines 47-55]; and

reading, when the LSI chip is returned from the standby state, the information held in the scanned information storage portion of the built-in storage section and setting the serial information through the scan path in the memory units of each of the circuits provided in the main power supply region [column 2, lines 23-27 and column 6, lines 47-55].

AAPA and Tobias do not explicitly teach converting the serial information into parallel information when storing the information into memory and converting the parallel information into serial information when reading the information from the memory. However, Goldstein states that serial/parallel conversion circuits are well known in the art to be used for converting a serial data stream to parallel in order to store the data in a memory and for converting parallel data to a serial data stream when reading the data from the memory [column 1, line 43 – column

2, line 3]. It would have been obvious to one of ordinary skill in the art to convert the serial data to parallel data when storing the data in memory because parallel data is easier to store in memory [Goldstein, column 1, lines 50-58].

Regarding claims 11 and 12, AAPA, Tobias and Goldstein, as described above, teach a method for reducing leakage current in an LSI chip. Tobias also teaches saving the scanned information in an external storage [external memory 200, column 7, lines 1-9].

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Tobias et al., US Patent no. 6,363,501 [Tobias], in view of, Masabumi et al., JP-A 5-108194[1] [Masabumi].

AAPA and Tobias do not explicitly teach controlling the substrate bias voltage of transistors while the LSI is in a standby state. However, the Applicant's specification states that controlling the substrate bias voltage of transistors in a circuit to reduce the leakage current while in a standby state, as described in Masabumi, is a well-known concept [page 22, paragraph 1]. Therefore, it would have been obvious to one of ordinary skill in the art to employ the well-known method taught by Masabumi in the LSI taught by AAPA and Tobias in order to reduce the power consumption of the LSI when it is operating in a standby state.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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[1] Included in IDS filed on 9/20/01

IEEE Standard Test Access Port and Boundary-Scan Architecture [IEEE 1149.1] discloses a standard for test access port and boundary-scan hardware.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
August 4, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100